REMARKS

Claims 1-30 are pending.

Claims 1, 9, 16, 22, and 25 are amended. No new subject matter is added. Claims 1-30 remain in the case for consideration. Reconsideration and allowance of claims 1-30 are requested in light of the above amendments and the following remarks.

Claim Rejections under 35 U.S.C. § 103

Claims 1-30 stand rejected under 35 USC 103(a) as being unpatentable over Erami in view of McCormick.

Claim 1 recites "a control processor to execute a control portion of link management; and a line processor to execute an offload portion of link management." Claims 9, 16, 22, and 25 recite similar features.

Erami teaches discovering the location of a failure of a data channel during a control channel failure in a transmission network system. Specifically, Erami discloses a first transmission device having a first failure detecting unit for detecting a failure of a working control channel; a second failure detecting unit for detecting a failure of a working data channel; a route searching unit for searching a route of a protection control channel; and a transmission unit for transmitting failure information detected by the second failure detecting unit to a second transmission device located at the upstream side via the protection control channel. *See* Erami, Col. 2, paragraph [0020], [0022], and abstract. Nowhere does Erami teach or suggest a control processor and a line processor respectively implementing a control portion and an offload portion of link management as recited in the claims 1, 9, 16, 22, and 25.

The Office Action acknowledges that Erami fails to disclose that each of the protocols is implemented in a control processor and a line processor respectively. *See* Office Action, page 10, third paragraph.

McCormick does not cure the deficiencies of Erami. McCormick discloses a multiprocessor control block, which includes a resource and routing processor 220, a plurality of intermediate processors 230-234, and a link layer processor 240. *See* McCormick, page 2, paragraph [0019]; and FIG. 3. McCormick further discloses that each of the processors in the multiprocessor control block perform functions associated with a protocol stack as illustrated in FIG. 4. *See* McCormick, page 2, paragraph [0019]; and FIG. 4. Specifically, the resource and routing processor 220 performs functions associated with resource distribution and routing 292 in the protocol stack of FIG. 4; the intermediate processors 230-234, each of which performs similar processing operations such as those included in the signaling link layer 295 of the protocol stack of FIG. 4 as well as call processing operations 293 of the protocol stack 290; and the link layer processor 240 performs functions included in the physical link layer 296 of the protocol stack 290. *See* McCormick, page 3, paragraphs [0020]-[0027]; and FIG. 4.

That is, McCormick teaches dividing a protocol stack consisting of multiple individual protocols on each layer of the stack among the processors of the multiprocessor control block, such that each processor would handle all of the functionalities associated with a protocol in the protocol stack. McCormick does not teach or suggest dividing *an individual protocol into a control portion and an offload portion among different processors*, such that "a control processor configured and arranged to execute a control portion of an interior gateway signaling protocol; and a line processor configured and arranged to execute an offload portion of an interior gateway signaling protocol." (Underline added).

Although McCormick mentions that multiple processors 230-234 may be used to perform call-processing operations for a corresponding portion of the connections supported by the communication switch, each intermediate processor performs similar processing operations, not different portions of a router control protocol, that is, a control portion and an offload portion of a router control protocol. *See* McCormick, page 3, paragraph [0027], lines 6-8. In fact, McCormick may use a single intermediate processor to perform all of the functionalities associated with call processing. *See* McCormick, page 3, paragraph [0024].

Claim 1, as amended, further recites "where the line processor is configured to aggregate information related to link failures, such that only one link failure notification is reported to the control card." Claims 9, 16, 22, and 25 recite similar features. *See* Specification, page 6, lines 1-5.

As discussed, neither Erami nor McCormick teach or suggest a distributed link management. As such, all link failure messages would be processed at a control processor, not "aggregate information related to link failures at the line card, such that only one link failure notification is sent to the control card" as specifically claimed.

For at least the reasons discussed above, claims 1-30 are therefore patentably distinguishable from Erami in view of McCormick. Claims 1-30 are in condition for allowance.

CONCLUSION

In view of the foregoing remarks, applicant believes the application should be in condition for allowance. If any questions remain, the Examiner is requested to call the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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